IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An information-handling system, comprising:

a plurality of processing elements; and

a plurality of memory sections, wherein each memory section comprises:

a memory array having a plurality of locations;

a memory interface operatively connecting the memory array to each of the processing elements; and

a plurality of processor translation look-aside buffers, wherein each processor translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements in order to translate addresses received from ~~the~~ its associated processing ~~elements~~ element, and wherein each processor translation look-aside buffer has a plurality of entries, each one of the plurality of entries being used to map a processor address received from its associated processing element into a memory array address of the memory array.

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~~2.~~ (Currently Amended) The information-handling system, comprising:

one or more memory sections, wherein each memory section comprises:

a memory array having a plurality of locations;

a memory interface operatively connecting the memory array to each of the processing elements, wherein the memory interface includes a FIFO; and

a plurality of processor translation look-aside buffers, wherein each processor translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements in order to translate addresses received from ~~the~~ its associated processing ~~elements~~ element, and wherein each processor translation look-aside buffer has a plurality of entries, each one of the plurality of entries being used to map a processor address received from its associated processing element into a memory array address of the memory array, wherein the FIFO accepts memory commands from two or more of the processing elements and transmits each of the memory commands to at least one of the processor translation look-aside buffers.

2 3. (Original) The information-handling system of claim 1, wherein the memory interface includes a plurality of FIFOs, wherein each FIFO is associated with one of the processing elements, and wherein each FIFO accepts memory commands from its associated processing element and transmits the memory commands to one of the processor translation look-aside buffers.

3 4. (Original) The information-handling system of claim 1, wherein the memory sections further include one or more I/O translation look-aside buffers, wherein each I/O translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements to translate addresses received from the processing element, and wherein each of the I/O translation look-aside buffers has a plurality of entries, each of the entries being used to map an I/O address into a memory array address of the memory array.

5. (Currently Amended) A method for addressing a memory within a memory system having two or more memory sections, including a first and a second memory section, wherein each memory section includes two or more translation look-aside buffers, the method comprising:

associating a translation look-aside buffer in each memory section with a first processor;

associating a different translation look-aside buffer in each memory section with a second processor;

routing a first memory command within the memory system to the first memory section, wherein the first memory command includes a first processor address;

mapping the first processor address into a first memory address using a the translation look-aside buffer associated with the first processor;

addressing memory data within the memory system with the first memory address;

routing a second memory command within the memory system, wherein the second memory command includes a second processor address;

mapping the second processor address into a second memory address using a the translation look-aside buffer associated with the second processor; and

addressing memory data within the memory system with the second memory array address.

6. (Original) The method of claim 5, wherein the routing of the first memory command includes processing the first memory command on a first in first out basis with regard to other memory commands.

7. (Original) The method of claim 5, wherein the second processor is an I/O processor.

8. (Previously Presented) An information-handling system comprising:

a memory having two or more memory sections, including a first and a second memory section, wherein each memory section includes two or more translation look-aside buffers; and

a plurality of processing elements, wherein each of the processing elements is operatively coupled to the memory;

wherein the memory includes mapping means for mapping processor addresses received from the processing elements into memory addresses in the memory, and wherein the mapping means includes a first translation look-aside buffer for translating processor addresses associated with a first processing element and a second translation look-aside buffer for translating processor addresses associated with a second processing element.

9-27. (Cancelled)

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28. (Currently Amended) The information-handling system of claim ~~1~~ 8, wherein the memory means includes a memory interface, wherein the memory interface includes a plurality of FIFOs, wherein each FIFO is associated with one of the processing elements, and wherein each FIFO accepts memory commands from its associated processing element and transmits the memory commands to one of the processor translation look-aside buffers.

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29. (Currently Amended) The information-handling system of claim ~~1~~ 8, wherein the memory sections further include one or more I/O translation look-aside buffers, wherein each I/O translation look-aside buffer is operatively coupled to the memory array and to one of the

processing elements to translate addresses received from the processing element, and wherein each of the I/O translation look-aside buffers has a plurality of entries, each of the entries being used to map an I/O address into a memory array address of the memory array.